What is claimed is:

1. A memory device, comprising:

a NOR architecture NROM memory array formed on a substrate having a plurality of pillars and associated intervening trenches; and

a plurality of memory cell structures, each memory cell structure comprising,

an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the NROM memory cell by a first source/drain region formed at the bottom of the trench.

2. The memory device of claim 1, further comprising:

a plurality of word lines, wherein each word line is coupled to one or more control gates of the NROM memory cells of the plurality of memory cell structures;

a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of memory cell structures;

at least one first bitline, wherein the at least one first bitline is coupled to one or more select gate drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures; and

at least one second bit line, wherein the at least one second bit line is coupled to one or more second source/drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures.

3. The memory device of claim 2, wherein the plurality of memory cell structures are formed into rows and columns such that each trench contains a cell structure and where the NROM memory cell and select gate of each memory cell structures of each row are arranged in an alternating pattern, such that each pillar

of the row has either two select gates or two NROM memory cells formed on opposing sidewalls.

4. An NROM memory cell structure, comprising:

a substrate, comprising two raised areas, defining a trench therebetween;

an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of the trench;

a select gate memory cell, wherein the select gate is formed vertically on a second sidewall of the trench; and

wherein the NROM memory cell is coupled to the select gate by source/drain regions at the bottom of the trench.

5. The NROM memory cell structure of claim 4, wherein the raised areas are pillars.

6. The NROM memory cell structure of claim 4, further comprising:

a word line, wherein the word line is coupled to a control gate of the NROM memory cell of the NROM memory cell structure;

a select line, wherein the select line is coupled to a control gate of the select gate of the NROM memory cell structure;

a first bitline, wherein the first bitline is coupled to a drain of the select gate; and

a second bitline, wherein the second bitline is coupled to a source/drain of the NROM memory cell.

7. An NROM memory array, comprising:

a substrate, comprising a plurality of pillars and associated intervening trenches; and

a plurality of memory cell structures, each memory cell structure comprising,

an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the NROM memory cell by a source/drain region formed at the bottom of the trench.

8. The NROM memory array of claim 7, further comprising:

a plurality of word lines, wherein each word line is coupled to one or more control gates of the NROM memory cells of the plurality of NROM memory cell structures;

a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of NROM memory cell structures;

at least one first bitline, wherein the at least one first bitline is coupled to one or more select gate drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and

at least one second bitline, wherein the at least one second bitline is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures.

9. The NROM memory array of claim 8, wherein the plurality of NROM memory cell structures are formed into rows and columns such that each trench contains an NROM memory cell structure and where the NROM memory cell and select gate of each NROM memory cell structure of each row is arranged in an alternating pattern, such that each pillar of the row has either two select gates or two NROM memory cells formed on opposing sidewalls.

10. The NROM memory array of claim 7, wherein the plurality of NROM memory cell structures are formed into rows and columns and an isolation region is formed between adjacent rows of NROM memory cell structures.

11. The NROM memory array of claim 10, wherein the isolation region is an oxide

insulator.

12. The NROM memory array of claim 7, wherein the plurality of NROM memory cell structures are formed into rows and columns and each row of NROM memory cell structures is formed on a separate P-well isolation region formed on the substrate.

13. A memory device comprising:

a NOR architecture NROM memory array formed on a substrate having a plurality of pillars and associated intervening trenches;

a plurality of NROM memory cell structures, each NROM memory cell structure comprising,

an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the NROM memory cell by a source/drain region formed at the bottom of the trench;

a control circuit;

a row decoder;

a plurality of word lines, wherein each word line is coupled to one or more control gates of the NROM memory cells of the plurality of NROM memory cell structures;

a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of NROM memory cell structures;

at least one first bit/data line, wherein the at least one first bit/data line is coupled to one or more select gate drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and

at least one second bit/data line, wherein the at least one bit/data line is coupled to one or more NROM memory cell source/drain regions formed at the top

of the plurality of pillars of the plurality of NROM memory cell structures.

14. A system, comprising:

a processor coupled to at least one memory device, wherein the at least one memory device comprises,

a NOR architecture NROM memory array formed on a substrate having a plurality of pillars and associated intervening trenches, and

a plurality of NROM memory cell structures, each NROM memory cell structure comprising,

an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the NROM memory cell by a source/drain region formed at the bottom of the trench.

15. A method of forming an NROM memory cell structure, comprising:

forming two raised areas on a substrate, the raised areas defining an associated intervening trench;

forming an NROM memory cell on a first sidewall of the trench;

forming a select gate on a second sidewall of the trench; and

forming a source/drain region at the bottom of the associated intervening trench.

16. The method of claim 15, wherein forming two raised areas on a substrate further comprises etching a trench in the substrate.

17. The method of claim 15, wherein forming two raised areas on a substrate further comprises forming two pillars on a substrate.

18. The method of claim 17, wherein forming two pillars on a substrate further comprises depositing additional substrate material on the substrate to form the two pillars.

19. The method of claim 15, wherein forming a source/drain region at the bottom of the associated intervening trench further comprises forming source/drain regions on the top of the two raised areas and at the bottom of the associated intervening trench in one of before the formation of the NROM memory cell and select gate and after the formation of the NROM memory cell and select gate.

20. The method of claim 15, wherein the substrate is P-doped.

21. The method of claim 15, wherein forming an NROM memory cell on a first sidewall of the trench and forming a select gate on a second sidewall of the trench further comprises forming an NROM transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall.

22. The method of claim 21, wherein forming an NROM transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall further comprises forming a tunnel insulator on the surface of the first sidewall, forming a trapping layer on the tunnel insulator, forming a first insulator as an intergate insulator over the trapping layer, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator.

23. The method of claim 21, wherein forming an NROM transistor gate-insulator stack on a surface of the first sidewall further comprises forming an NROM transistor gate-insulator stack of one of oxide-nitride-oxide (ONO), oxide-

nitride-aluminum oxide, oxide-aluminum oxide-oxide, oxide-silicon oxycarbide-oxide, composite layers of an oxide-an oxide of Ti, Ta, Hf, Zr, or La, and an oxide, composite layers of an oxide-a non-stoichiometric oxide of Si, N, Al, Ti, Ta, Hf, Zr, and La, and an oxide, composite layers of an oxide-a wet oxide not annealed, and an oxide, composite layers of an oxide-a silicon rich oxide, and an oxide, composite layers of an oxide-a silicon rich aluminum oxide, and an oxide, and composite layers of an oxide-a silicon oxide with silicon carbide nanoparticles, and an oxide.

24. The method of claim 22, wherein forming a tunnel insulator on the surface of the first sidewall, forming a trapping layer on the tunnel insulator, forming a first insulator as an intergate insulator over the trapping layer, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator further comprises first forming a tunnel insulator on the surface of the first sidewall and forming a trapping layer on the tunnel insulator, then forming the first and second insulators over the trapping layer and on the surface of the second sidewall, and forming the first and second control gates over the first and second insulators, wherein each layer is deposited over the two raised areas and trench, masked, and directionally etched.

25. A method of forming a floating gate memory array, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate by depositing a layer of masking material, patterning the masking material, and anisotropically etching the substrate; and

forming a plurality of NROM memory cell structures, each NROM memory cell structure having a trapping layer and a coupled select gate, where each NROM memory cell structure is formed by,

depositing a layer of tunnel insulator material over two pillars and an intervening trench;

masking and anisotropically etching the layer of tunnel insulator material to form a tunnel insulator of an NROM memory cell on a first sidewall of the trench;

depositing a layer of trapping layer material over the two pillars and intervening trench;

masking and anisotropically etching the layer of trapping layer material to form a trapping layer on the tunnel insulator on the first sidewall of the trench;

depositing a layer of gate insulator material over the two pillars and intervening trench;

masking and anisotropically etching the layer of gate insulator material to form a first gate insulator on the trapping layer on the first sidewall and a second gate insulator of a select gate on a second sidewall of the trench;

depositing a layer of gate material over the two pillars and intervening trench;

masking and anisotropically etching the layer of gate material to form a first and second control gates on the first and second gate insulators on the first and second sidewalls of the trench; and

diffusing a dopant material into the bottom of the trench and the tops of the two pillars to form source/drain regions of the select gate and the NROM memory cell.

26. The method of claim 25, further comprising:

forming the plurality of NROM memory cell structures into rows; and

forming an isolation region between adjacent rows of NROM memory cell structures by depositing an oxide insulator between adjacent rows.

27. A method of forming an NROM memory array, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate; and

forming a plurality of NROM memory cell structures, each NROM memory cell structure is formed by,

forming an NROM memory cell on a first sidewall of a trench;

forming a select gate on a second sidewall of the trench; and

forming a source/drain region at the bottom of the trench.

28. The method of claim 27, wherein the substrate is P-doped.

29. The method of claim 27, further comprising:

forming the plurality of NROM memory cell structures into rows; and

forming a P-well isolation region under each row of NROM memory cell structures.

30. The method of claim 27, further comprising:

forming the plurality of NROM memory cell structures into rows; and

forming an isolation region between adjacent rows of NROM memory cell structures.

31. The method of claim 30, wherein forming an isolation region between adjacent rows of vertical NOR architecture NROM memory cell structures further comprises forming an isolation region of an oxide insulator.

32. The method of claim 30, further comprising:

forming a plurality of word lines across the isolation region between adjacent rows of NROM memory cell structures, wherein each word line is coupled to a control gate of a single NROM memory cell of each row of NROM memory cell structures.

33. The method of claim 30, further comprising:

forming a plurality of select lines across the isolation region between adjacent rows of NROM memory cell structures, wherein each select line is coupled to a control gate of a single select gate of each row of NROM memory cell structures.

34. The method of claim 27, wherein forming an NROM memory cell on a first sidewall of the trench and forming a select gate on a second sidewall of the trench further comprises forming an NROM transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall.

35. The method of claim 34, wherein forming an NROM transistor gate-insulator stack on a surface of the first sidewall further comprises forming an NROM transistor gate-insulator stack of one of oxide-nitride-oxide (ONO), oxide-nitride-aluminum oxide, oxide-aluminum oxide-oxide, oxide-silicon oxycarbide-oxide, composite layers of an oxide-an oxide of Ti, Ta, Hf, Zr, or La, and an oxide, composite layers of an oxide-a non-stoichiometric oxide of Si, N, Al, Ti, Ta, Hf, Zr, and La, and an oxide, composite layers of an oxide-a wet oxide not annealed, and an oxide, composite layers of an oxide-a silicon rich oxide, and an oxide, composite layers of an oxide-a silicon rich aluminum oxide, and an oxide, and composite layers of an oxide-a silicon oxide with silicon carbide nanoparticles, and an oxide.

36. The method of claim 34, wherein forming an NROM transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall further comprises forming a tunnel insulator on the surface of the first sidewall, forming a trapping layer on the tunnel insulator, forming a first insulator as an intergate insulator over the trapping layer, and forming a first control gate over the first insulator, and on the

surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator.

37. The method of claim 36, wherein forming a tunnel insulator on the surface of the first sidewall, forming a trapping layer on the tunnel insulator, forming a first insulator as an intergate insulator over the trapping layer, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator further comprises first forming a tunnel insulator on the surface of the first sidewall and forming a trapping layer on the tunnel insulator, then forming the first and second insulators over the trapping layer and on the surface of the second sidewall, and forming the first and second control gates over the first and second insulators, wherein each layer is deposited over the trench, masked, and directionally etched in combined layers to produce the NROM and select gate gate-insulator stacks.

38. The method of claim 27, further comprising:

forming at least one first bit/data line, wherein the at least one first bit/data line is coupled to one or more select gate drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and

forming at least one second bit/data line, wherein the at least one second bit/data line is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures.

39. The method of claim 27, wherein forming a plurality of NROM memory cell structures further comprises forming a plurality of NROM memory cell structures, wherein the plurality of NROM memory cell structures are formed into rows and where the NROM memory cell and select gate of each NROM memory cell structure of each row is formed in an alternating pattern, such that

each pillar of the row has either two select gates or two NROM memory cells formed on its sidewalls.

40. A method of forming an NROM EEPROM memory device, comprising:
forming a plurality of pillars and associated intervening trenches on a substrate;
forming a plurality of NROM memory cells on a first sidewall of each trench;
forming a plurality of select gates on a second sidewall of each trench; and
forming one or more source/drain regions on the top of the plurality of pillars and at the bottom of the associated intervening trenches.

41. A NAND architecture NROM memory cell string, comprising:
a substrate, comprising one or more raised areas, defining trenches therebetween;
a plurality of NROM memory cells, wherein the NROM memory cells are formed vertically on the sidewalls of the trenches;
wherein the plurality of NROM memory cells are coupled in a serial string by source/drain regions formed at the top of the one or more raised areas and at the bottom of the one or more trenches; and
wherein a first NROM memory cell of the string is coupled to a first select gate.

42. The NROM memory cell string of claim 41, wherein a last NROM memory cell of the string is coupled to a second select gate.

43. The NROM memory cell string of claim 41, wherein the raised areas are pillars.

44. The NROM memory cell string of claim 42, further comprising:
a plurality of word lines, wherein each word line is coupled to a control gate of an NROM memory cell of the string;
one or more select lines, wherein each select line is coupled to a control gate of a select gate of the string;

a first bitline, wherein the first bitline is coupled to a source/drain of the first select gate; and

a second bitline, wherein the second bitline is coupled to a source/drain of the second select gate of the string.

45. A memory array, comprising:

a substrate, comprising a plurality of pillars and associated intervening trenches;

a plurality of NROM memory cells, wherein the NROM memory cells are formed vertically on the sidewalls of the plurality of pillars and trenches;

wherein the plurality of NROM memory cells are coupled into a plurality of NAND architecture memory strings by source/drain regions formed at the top of the plurality of pillars and at the bottom of the associated trenches; and

wherein a first NROM memory cell of each NAND architecture memory string is coupled to a first vertical select gate and a last NROM memory cell of each NAND architecture memory string is coupled to a second vertical select gate.

46. The memory array of claim 45, further comprising:

a plurality of word lines, wherein each word line is coupled to one or more control gates of one or more NROM memory cells, where each of the one or more NROM memory cells is from a differing memory string;

a plurality of select lines, wherein each select line is coupled to one or more select gates;

at least one first bitline, wherein the at least one first bitline is coupled to a source/drain of the first select gate of each memory string; and

at least one second bitline, wherein the at least one second bitline is coupled to a source/drain of the second select gate of each memory string.

47. The memory array of claim 45, wherein an isolation region is formed between

adjacent memory strings.

48. A memory device, comprising:

a memory array formed on a substrate having a plurality of pillars and associated intervening trenches;

a plurality of NROM memory cells, wherein the NROM memory cells are formed vertically on the sidewalls of the plurality of pillars and trenches;

wherein the plurality of NROM memory cells are coupled into a plurality of NAND architecture memory strings by source/drain regions formed at the top of the plurality of pillars and at the bottom of the associated trenches; and

wherein a first NROM memory cell of each string is coupled to a first select gate and a last NROM memory cell of each string is coupled to a second select gate.

49. The memory device of claim 48, further comprising:

a plurality of word lines, wherein each word line is coupled to one or more control gates of one or more NROM memory cells, where each of the one or more NROM memory cells is from a differing string;

a plurality of select lines, wherein each select line is coupled to one or more select gates;

at least one first bit/data line, wherein the at least one first bit/data line is coupled to a source/drain of the first select gate of each string; and

at least one second bit/data line, wherein the at least one second bit/data line is coupled to a source/drain of the second select gate of each string.

50. A memory device comprising:

a NAND architecture memory array formed on a substrate having a plurality of pillars and associated intervening trenches;

a plurality of NROM memory cells, wherein the NROM memory cells are

formed vertically on the sidewalls of the plurality of pillars and trenches;

wherein the plurality of NROM memory cells are coupled into a plurality of NAND architecture memory strings by source/drain regions formed at the top of the plurality of pillars and at the bottom of the associated trenches;

wherein a first NROM memory cell of each string is coupled to a first vertical select gate and a last NROM memory cell of each string is coupled to a second vertical select gate;

a control circuit;

a row decoder;

a plurality of word lines coupled to the row decoder, wherein each word line is coupled to one or more control gates of one or more NROM memory cells, where each of the one or more NROM memory cells is from a differing string;

a plurality of select lines, wherein each select line is coupled to one or more select gates;

at least one first bitline, wherein the at least one first bitline is coupled to a source/drain of the first select gate of each string; and

at least one second bitline, wherein the at least one second bitline is coupled to a source/drain of the second select gate of each string.

51. A system, comprising:

a processor coupled to at least one memory device, wherein the at least one memory device comprises,

a memory array formed on a substrate having a plurality of pillars and associated intervening trenches,

a plurality of NROM memory cells, wherein the NROM memory cells are formed vertically on the sidewalls of the plurality of pillars and trenches,

wherein the plurality of NROM cells are coupled into a plurality of NAND architecture memory strings by source/drain regions formed at the top of

the plurality of pillars and at the bottom of the associated trenches, and

wherein a first NROM memory cell of each string is coupled to a first vertical select gate and a last NROM memory cell of each string is coupled to a second vertical select gate.

52. A memory device comprising:

a memory array formed on a substrate having a plurality of NROM memory cells arranged in rows and columns and coupled into a plurality of NAND memory strings, wherein the NROM memory cells are formed vertically on the sidewalls of the plurality of pillars and associated trenches formed on the substrate, and where the plurality of NROM cells are coupled into the plurality of NAND memory strings by source/drain regions formed at the top of the plurality of pillars and at the bottom of the associated trenches;

wherein a first NROM memory cell of each string is coupled to a first vertical select gate and a last NROM memory cell of each string is coupled to a second vertical select gate;

a plurality of word lines, wherein each word line is coupled to one or more gates of a row of the NROM memory cells;

a plurality of select lines, wherein each select line is coupled to one or more select gates;

at least one first bitline, wherein the at least one first bitline is coupled to a source/drain of the first select gate of each string; and

at least one second bitline, wherein the at least one second bitline is coupled to a source/drain of the second select gate of each string.

53. A method of forming a NAND architecture memory cell string, comprising:

forming one or more raised areas on a substrate, the raised areas defining associated intervening trenches;

forming a plurality of NROM memory cells on the sidewalls of the one or more raised areas;

forming one or more source/drain regions on the top of the one or more raised areas and at the bottom of the one or more associated intervening trenches; and

forming a first vertical select gate coupled to a first NROM memory cell of the string and a second vertical select gate coupled to a last NROM memory cell of the string.

54. The method of claim 53, wherein forming one or more raised areas on a substrate further comprises etching a trench in the substrate.

55. The method of claim 53, wherein forming one or more raised areas on a substrate further comprises forming one or more pillars on a substrate.

56. The method of claim 55, wherein forming one or more raised areas on a substrate further comprises depositing additional substrate material on the substrate to form the one or more pillars.

57. The method of claim 53, wherein forming one or more source/drain regions on the top of the one or more raised areas and at the bottom of the one or more associated intervening trenches further comprises forming one or more source/drain regions on the top of the one or more raised areas and at the bottom of the one or more associated intervening trenches in one of before the formation of the plurality of NROM memory cells and after the formation of the plurality of NROM memory cells.

58. The method of claim 53, wherein forming a plurality of NROM memory cells on the sidewalls of the one or more raised areas and forming a first vertical select gate coupled to a first NROM memory cell of the NAND architecture memory string and a second vertical select gate coupled to a last NROM memory cell of the NAND architecture memory string further comprises forming an NROM

gate-insulator stack on the surface of a first plurality of selected sidewalls and forming a first and second select gate gate-insulator stack on the surface of a second plurality of selected sidewalls.

59. The method of claim 58, wherein forming a plurality of NROM gate-insulator stack on the surface of the first plurality of selected sidewalls further comprises forming an NROM gate-insulator stack of one of oxide-nitride-oxide (ONO), oxide-nitride-aluminum oxide, oxide-aluminum oxide-oxide, oxide-silicon oxycarbide-oxide, composite layers of an oxide-an oxide of Ti, Ta, Hf, Zr, or La, and an oxide, composite layers of an oxide-a non-stoichiometric oxide of Si, N, Al, Ti, Ta, Hf, Zr, and La, and an oxide, composite layers of an oxide-a wet oxide not annealed, and an oxide, composite layers of an oxide-a silicon rich oxide, and an oxide, composite layers of an oxide-a silicon rich aluminum oxide, and an oxide, and composite layers of an oxide-a silicon oxide with silicon carbide nanoparticles, and an oxide.

60. The method of claim 58, wherein forming a plurality of NROM memory cells on the sidewalls of the one or more raised areas by forming an NROM gate-insulator stack on the surface of a first plurality of selected sidewalls and forming a first and second vertical select gate gate-insulator stack on the surface of a second plurality of selected sidewalls further comprises forming a tunnel insulator on the surface of the first plurality of selected sidewalls, forming a trapping layer on the tunnel insulator, forming a first insulator as an intergate insulator over the trapping layer, and forming a first control gate over the first insulator, and on the surface of the second plurality of selected sidewalls forming a second insulator and forming a second control gate over the second insulator.

61. The method of claim 60, wherein forming a tunnel insulator on the surface of the first plurality of selected sidewalls, forming a trapping layer on the tunnel

insulator, forming a first insulator as an intergate insulator over the trapping layer, and forming a first control gate over the first insulator, and on the surface of the second plurality of sidewalls forming a second insulator and forming a second control gate over the second insulator further comprises first forming a tunnel insulator on the surface of the first plurality of selected sidewalls and forming a trapping layer on the tunnel insulator, then forming the first and second insulators over the trapping layer of the first plurality of selected sidewalls and on the surface of the second plurality of selected sidewalls, and forming the first and second control gates over the first and second insulators, wherein each layer is deposited over the two raised areas and trench, masked, and directionally etched.

62. A method of forming a NAND architecture memory array, comprising:
forming a plurality of pillars and associated intervening trenches on a substrate;
forming a plurality of vertical NROM memory cells on a first plurality of selected sidewalls of the plurality of pillars;
forming a plurality of select gates on a second plurality of selected sidewalls of the plurality of pillars; and
forming one or more source/drain regions on the top of the plurality of pillars and at the bottom of the associated intervening trenches to form a plurality of NAND architecture memory strings.

63. The method of claim 62, further comprising:
forming a P-well isolation region under each memory string.

64. The method of claim 62, further comprising:
forming an isolation region between adjacent memory strings.

65. The method of claim 64, further comprising:

forming a plurality of word lines and a plurality of select lines across the isolation region between adjacent memory strings, wherein each word line is coupled to a control gate of a single NROM memory cell of each memory string and each select line is coupled to a select gate of each memory string.

66. The method of claim 62, wherein forming a plurality of vertical NROM memory cells on the first plurality of selected sidewalls and forming a plurality of select gates on a second plurality of selected sidewalls further comprises forming an NROM gate-insulator stack on the surface of the first plurality of selected sidewalls and forming a select gate gate-insulator stack on the surface of the second plurality of selected sidewalls.

67. The method of claim 66, wherein forming an NROM gate-insulator stack on the surface of the first plurality of selected sidewalls further comprises forming an NROM gate-insulator stack of one of oxide-nitride-oxide (ONO), oxide-nitride-aluminum oxide, oxide-aluminum oxide-oxide, oxide-silicon oxycarbide-oxide, composite layers of an oxide-an oxide of Ti, Ta, Hf, Zr, or La, and an oxide, composite layers of an oxide-a non-stoichiometric oxide of Si, N, Al, Ti, Ta, Hf, Zr, and La, and an oxide, composite layers of an oxide-a wet oxide not annealed, and an oxide, composite layers of an oxide-a silicon rich oxide, and an oxide, composite layers of an oxide-a silicon rich aluminum oxide, and an oxide, and composite layers of an oxide-a silicon oxide with silicon carbide nanoparticles, and an oxide.

68. The method of claim 66, wherein forming an NROM gate-insulator stack on the surface of the first plurality of selected sidewalls and forming a select gate gate-insulator stack on the surface of the second plurality of selected sidewalls further comprises forming a tunnel insulator on the surface of the first plurality of selected sidewalls, forming a trapping layer on the tunnel insulator, forming an intergate insulator over the trapping layer, and forming a control gate over the

intergate insulator and forming an insulator on the surface of the second plurality of selected sidewalls and forming a control gate over the insulator.

69. A method of forming a memory device, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate;

forming a plurality of vertical NROM memory cells on a first plurality of selected sidewalls of the plurality of pillars;

forming a plurality of select gates on a second plurality of selected sidewalls of the plurality of pillars; and

forming one or more source/drain regions on the top of the plurality of pillars and at the bottom of the associated intervening trenches to form a plurality of NAND architecture memory strings.

70. A method of forming an NROM NAND architecture memory cell string, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate by depositing a layer of masking material, patterning the masking material, and anisotropically etching the substrate; and

forming a NAND architecture NROM memory cell string having a plurality of NROM memory cells and one or more select gates, where the string is formed by,

depositing a layer of tunnel insulator material over the plurality of pillars and intervening trenches;

masking and anisotropically etching the layer of tunnel insulator material to form a tunnel insulator of an NROM memory cell on a first selected number of sidewalls of the pillars;

depositing a layer of trapping layer material over the plurality of pillars and intervening trenches;

masking and anisotropically etching the layer of trapping layer material to form a trapping layer on the tunnel insulator on the first selected number

of sidewalls;

depositing a layer of gate insulator material over the plurality of pillars and intervening trenches;

masking and anisotropically etching the layer of gate insulator material to form a gate insulator on the NROM memory cells on the first selected number of sidewalls and gate insulator of a select gate on a second selected number of sidewalls of the pillars;

depositing a layer of gate material over the plurality of pillars and intervening trenches; and

masking and anisotropically etching the layer of gate material to form a control gate on the gate insulator material the first and second selected numbers of sidewalls.

71. The method of claim 70, further comprising:

diffusing a dopant material into the bottom of each trench and the top of each pillar to form source regions and drain regions of the one or more select gates and the plurality of NROM memory cells.